**IR3889**

**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Features**

∙ Single 4.3 V to 17 V application or Wide Input Voltage Range from 2.0 V to 17 V with an External VCC ∙ Precision Reference Voltage (0.8 V +/- 0.5%)

∙ Enhanced Fast COT Engine Stable with Ceramic Output Capacitors

∙ Optional Forced Continuous Conduction Mode and Diode Emulation for Enhanced Light Load Efficiency ∙ Programmable Switching Frequency from 600 kHz to 2 MHz

∙ Monotonic Start-Up with Four Selectable Soft-Start Time & Enhanced Pre-Bias Start-Up ∙ Thermally Compensated Internal Over Current Protection with Four Selectable Settings ∙ Enable input with Voltage Monitoring Capability & Power Good Output

∙ Thermal Shut Down

∙ Operating Temp: -40 °C < Tj < 125 °C

∙ Small Size: 5 mm x 6 mm PQFN

∙ Halogen-free and RoHS2 Compliant with Exemption 7a

**Potential applications**

∙ Server Applications

∙ Storage Applications

∙ Telecom & Datacom Applications

∙ Distributed Point of Load Power Architectures

**Product validation**

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

**Description**

The IR3889 is an easy-to-use, fully integrated dc - dc Buck regulator. The onboard PWM controller and OptiMOS™ FETs with integrated bootstrap diode make IR3889 a small footprint solution, providing high-efficient power delivery. Furthermore, it uses a fast Constant On-Time (COT) control scheme, which simplifies the design efforts and achieves fast control response.

The IR3889 has an internal low dropout voltage regulator, allowing operations with a single supply. It can also operate with an external bias supply, with an extended operating input voltage (PVin) range from 2.0 V to 17 V.

The IR3889 is a versatile regulator, offering programmable switching frequency from 600 kHz to 2 MHz, four selectable current limits, four selectable soft-start time, Forced Continuous Conduction Mode (FCCM) and Diode Emulation Mode (DEM) operation.

It also features important protection functions, such as pre-bias start-up, thermally compensated current limit, over voltage and under voltage protection, and thermal shutdown to give required system level security in the event of fault conditions.

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**Ordering information**

**1 Ordering information**

**1. Ordering Information**

| **Package Type** | **Standard Pack Form and Qty** | |
| --- | --- | --- |
| QFN 5 mm x 6 mm | Tape and Reel | 5000 |

**Sales Product Name Orderable Part Number** IR3889MTRPBF IR3889MTRPBFAUMA1

| IR3889MTRPBF  A1  Designator  Packing type Tape & Reel  Moisture  protection packing Dry  UM  Packing size 330 mm  Halogen Free Yes  A  RoHS compliant Yes  Total lead free No |
| --- |

| VSENM FBSS/Latch TON/MODE NC NCNCAGND  36 35 34 33 32 31 30 29  NC  ILIM  1  28  PGood  En  2  27  BOOT  Vin  26  3  VCC/LDO  PHASE  25  4  PVin  VDRV  5  24  GATEL  37  GATEL  PVin  6  23  PGND  22  PVin  7  PGND  PVin  21  8  PGND  PVin  20  9  PGND  PGND  10  19  11 12 13 14 15 16 17 18  SW SW SW SW SW SW SW SW |
| --- |

**Figure 1 Package Top View**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator Functional block diagram**

**2 Functional block diagram**

| **VCC/LDO**  **VDRV**  **AGND**  **PGood Vin**  **AGND**  **POR**  **UVP**  **UVP**  **OTP**  **Threshold**  +  **ENLDO**  **VCC**  -  **Fault**  **AGND**  **BOOT**  **OVP**  +  -**Hysteresis**  **OVP**  **Turn-on Delay**  **Threshold**  **PVin**  **PGood**  S **Prebias**  Q  **HDrVin**  **HDrv**  R  Q  **Fault**  +  -  **PGood**  **Hysteresis**  **Threshold**  **PHASE**  **POR**  +  **VCC**  **GATE**  **Hiccup**  **POR**  -  **4.0V**  **DRIVE**  **SW**  **OVP**  **LOGIC**  **VDRV**  **OTP**  **En**  +  **Fault**  **1.2V**  -  **LDrVin LDrv**  **PWM**  **PWM**  **COMP**  **SOFT**  **SS**  **SS/Latch**  **ADAPTIVE**  **+**  **START**  **SET**  **ON-TIME**  **-**  **ZC**  **PGND**  **-**  **GENERATOR**  **+**  **Zero Cross**  **PGND**  **DETECTION SW**  **FB**  **GATEL**  **RAMP**  **OCP**  +  **OVP**  **Floor**  **GENERATOR**  **Latch Off**  **GENERATOR**  **Hiccup**  **VSENM** - +    S  Q  **UVP**  **VREF**  R  **TON/**  **SW**  **MODE**  **20ms**  **Delay**  **ILIM** |
| --- |

**Figure 2 Block diagram**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Typical application diagram**

**3 Typical application diagram**

| PVin  Enable  EN Vin PVin  BOOT  VCC/LDO  PHASE  VDRV Vo  SW  PGood  0.1uF  NC  IR3889  PGood  GATEL  SS/Latch  FB  TON/MODE  Cff  ILIM VSENM  NC NC NC  AGND PGND  RFB1  RFB2 |
| --- |

**Figure 3 IR3889 basic application circuit**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator Pin descriptions**

**4 Pin descriptions**

Note: I = Input, O = Output

| **Pin Name** | **I/O** | **Type** |
| --- | --- | --- |
| ILIM | I | Analog |
| PGood | O | Analog |
| Vin | I | Power |
| VCC/LDO | I/O | Power |
| VDRV | I | Power |
| GATEL | I | Analog |
| PGND | - | Ground |
| SW | O | Power |
| PVin | I | Power |
| PHASE | O | Analog |
| BOOT | I | Analog |
| En | I | Analog |
| SS/Latch | I | Analog |

**Pin# Pin Description** Connecting a resistor to a quiet ground to set the Over

1

2

3

4

5

6, 37

7, 8, 9, 10, 19

11, 12, 13, 14, 15, 16, 17, 18

20, 21, 22,

Current Protection (OCP) limit. Four user selectable OCP limits are available.

Power Good status output pin is open drain. Connect a pull up resistor from this pin to VCC or to an external bias voltage, e.g. 3.3 V.

Input voltage for an Internal LDO. A 4.7 µF capacitor should be connected between this pin and PGND. If an external supply is connected to VCC/LDO pin, this pin should be shorted to VCC/LDO pin and a 10 µF ceramic capacitor can be shared with Vin and VCC/LDO pin.

Output of the internal LDO or input for an external VCC voltage. A 2.2 µF - 10 µF ceramic capacitor is recommended to use between VCC, VDRV and the Power ground (PGND). Input bias for the internal driver. It should be shorted to VCC/LDO pin on the PCB. A 2.2 µF - 10 µF ceramic capacitor is recommended to use between VDRV, VCC/LDO and the Power ground (PGND).

Gate of Low-side FET. This pin can be used to monitor the gate signal of LS FET. No external components should be connected to it.

Power Ground. Must be connected to the system’s power ground plane. PGND and AGND are internally connected via the lead frame.

Switch Node. Connect these pins to an output inductor.

23, 24 Input supply for the power stage. Source of High-side FET. Connect a bootstrap capacitor

between this pin and BOOT pin. A high temperature (x7R) 0.1

25

µF or greater value ceramic capacitor is recommended.

Supply voltage for the high side driver. Connect this pin to

the PHASE pin through a bootstrap capacitor. For PVin above

14 V, a resistor (e.g., 1 Ω~у ΩҚ is recommended in series with

26

the bootstrap capacitor to control the slew rate of the SW

node rising edge.

27 Enable pin to turn the IC on and off. Multi-function pin. Connect a resistor to a quiet ground to

select Soft-Start time from 4 options. This pin also selects

29

latched-off Over Voltage Protection (OVP) or non-latched

OVP.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Pin descriptions**

| **Pin Name** | **I/O** | **Type** |
| --- | --- | --- |
| FB | I | Analog |
| VSENM | - | Analog |
| AGND | - | Ground |
| TON/MODE | I | Analog |
| NC | - | Not  connected |

**Pin# Pin Description** Output voltage feedback pin. Connect this pin to the output

of the regulator via a resistor divider to set the output

30

voltage.

This pin provides the return connection for a pseudo remote

voltage sensing. The feedback resistor divider should be

31

connected to this pin. It is also used as ground for the

internal reference voltage.

32 Signal ground for the internal circuitry except the internal reference voltage.

Multi-function pin. Connect a resistor to a quiet ground to set

36

28, 33, 34,

the switching frequency to 1 of 8 settings and sets the mode of operation to FCCM or DEM.

35 Not connected internally. They can be left floating on PCB.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Absolute maximum ratings**

**5 Absolute maximum ratings**

**Absolute maximum ratings**

| **Min** | **Max** | **Unit** |
| --- | --- | --- |
| -0.3 | 25 | V |
| -0.3 V(dc) ,  below -5 V for 5 ns | 25 V(dc),  above 32 V for 2 ns | V |
| -0.3 | 6 | V |
| -0.3 V(dc),  below -0.3 V for 5 ns | 29 | V |
| -0.3 (dc),  below -5 V for 5 ns | 25 V(dc),  above 32 V for 2 ns | V |
| -0.3 | 6 V(dc),  7 V for 5 ns | V |
| -0.3 | 6 | V |
| -0.3 | 0.3 | V |
| -0.3 | 0.3 | V |
| -55 | 150 | °C |
| -40 | 150 | °C |

**Description Conditions** PVin, Vin, En to PGND Note **1** PVin to SW and PHASE

VCC, VDRV to PGND Note **1** BOOT to PGND Note **1**

SW and PHASE to PGND Note **1** BOOT to PHASE

ILIM, FB, PGood, TON/MODE,

GATEL and SS to AGND Note **1** PGND to AGND

VSENM to AGND

Storage Temperature Range

Junction Temperature Range

Note:

1. PGND, VSENM, and AGND pin are connected together

**Attention: Stresses beyond these listed under ȊAbsolute Maximum Ratingsȋ may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Thermal Characteristics**

**6 Thermal Characteristics**

**6.1 Thermal Characteristics**

| **Symbol** | **Values** |
| --- | --- |
| θJA | 19 °C/W |
| θJC-PCB | 1.1 °C/W |
| θJC | 24 °C/W |

**Description Test Conditions** Junction to Ambient Thermal Resistance Note **2** Junction to PCB Thermal Resistance Note **3** Junction to Case Top Thermal Resistance

Note:

2. Thermal resistance is measured with components mounted on a standard EVAL\_3889\_1Vout demo board in free air.

3. Thermal resistance is based on the board temperature near the pin 22.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Electrical specifications**

**7 Electrical specifications**

**7.1 Recommended operating conditions**

| **Min** | **Max** | **Unit** |
| --- | --- | --- |
| 2 | 17 | V |
| 4.5 | 17 | V |
| 4.3 | 5.5 | V |
| 0.8 | 6 | V |
|  | 30 | A |
| 600 | 2000 | kHz |
| -40 | 125 | °C |

**Description Note**

PVin Voltage Range with External VCC Note **4**, Note **5** PVin Voltage Range with Internal LDO Note **5**, Note **6 & 10** VCC and VDRV Supply Voltage Range Note **4**, Note **7** Output Voltage Range Note **8**, Note **9** Continuous Output Current Range Note **9** Switching Frequency Note **10** Operating Junction Temperature

Note:

4. Vin is shorted to VCC and use an external bias voltage.

5. A common practice is to have 20% margin on the maximum SW node voltage in the design. For applications requiring PVin equal to or above 14 V, a small resistor in series with the Boot pin should be used to ensure the maximum SW node spike voltage does not exceed 20 V. Alternatively, a RC snubber can be used at the SW node to reduce the SW node spike.

6. Vin is connected to PVin and the internal LDO is used. For single-rail applications with the internal LDO and PVin =Vin = 4.3 V-5.4 V, the internal LDO may enter dropout mode. OCP limits can be reduced due to the lower VCC voltage. Please refer to **Section 12.7** for more detailed design guidelines.

7. The IR3889 is designed to function with VCC down to 4.2 V, however, electrical specifications such as OCP limits may be degraded.

8. The maximum output voltage is also limited by the minimum off-time. Please refer to **Section 12.13** for details. Also note that OCP limit may be degraded when off-time is close to the minimum off-time. 9. Refer to **Section 9** for maximum output current rating at different ambient temperatures. 10. The maximum LDO output current must be limited within 50 mA for operations requiring full operating temperature range of -40 °C ൑ TJ ൑ 125 °C. **Figure 6** shows the maximum LDO output current capability over junction temperature. Thermal de-rating may be needed at an elevated ambient temperature to ensure the junction temperature within the recommended operating range.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator Electrical specifications**

**7.2 Electrical characteristics**

Note: Unless otherwise specified, the specifications apply over 4.5 V ≤ Vin = PVin ≤ ǖ7 V, Ǖ °C < TJ < 125 °C. Typical values are specified at Ta = 25 °C.

| **Symbol** | **Conditions** | **Min** | **Typ** | **Max** |
| --- | --- | --- | --- | --- |

**Parameter Unit Power Stage**

| Rds(on)\_Top | VBoot – Vsw= 5.0 V, IO = 30 A, Tj =25 °C |  | 2.4 |  |
| --- | --- | --- | --- | --- |
| Rds(on)\_Bot | VCC = 5.0 V, Io = 30 A, Tj =25 °C |  | 0.8 |  |
|  | I(BOOT) = 25 mA |  | 280 | 600 |
| VSW | En = 0 V |  |  | 300 |
| En = high, No Switching |  |  | 300 |
| Tdb | SW node falling edge, Io = 30 A, Internal LDO, Tj = 25 °C, Note **11** |  | 10 |  |
| SW node rising edge, Io = 30 A, Internal LDO, Tj = 25 °C, Note **11** |  | 5 |  |

Top Switch mΩ Bottom Switch

Bootstrap Forward Voltage mV SW float voltage mV

ns

Dead Band Time

ns

**Supply Current**

| Iin(Standby) | En = Low, No Switching |  | 4 | 10 |
| --- | --- | --- | --- | --- |
| Iin(Static) | En=2 V, No Switching |  | 2.3 | 4 |

Vin Supply Current (standby) µA Vin Supply Current (static) mA **Soft Start**

| SS rate | SS/Latch = 0 kΩ, 4.53 kΩ,  10.5 kΩ, 18.7 kΩ; | 0.4 | 0.8 | 1.12 |
| --- | --- | --- | --- | --- |
| SS/Latch =1.5 kΩ, 5.76 kΩ,  12.1 kΩ, 21.5 kΩ; | 0.2 | 0.4 | 0.56 |
| SS/Latch = 2.49 kΩ, 7.32 kΩ,  14 kΩ, 24.9 kΩ, Floating | 0.1 | 0.2 | 0.28 |
| SS/Latch = 3.48 kΩ, 8.87 kΩ,  тч.у kΩ, ущ.ш kΩ; | 0.05 | 0.1 | 0.145 |

Soft Start Ramp Rate mV/μs

**Feedback Voltage**

| VFB |  |  | 0.8 |  |
| --- | --- | --- | --- | --- |
|  | 0°C < Tj < 85 °C | -0.5 |  | +0.5 |
| -40 °C < Tj < 125 °C, Note **12** | -1 |  | 1 |
| IVFB | VFB=0.8 V, Tj=25 °C | -150 | 0 | +150 |

Feedback Voltage V Accuracy%

VFB Input Current nA **On-Time Timer Control**

| Ton | Vin=12 V, Vo=1 V,  TON= с kΩ or тс.ц kΩ, Note **13** |  | 151 |  |
| --- | --- | --- | --- | --- |
| Vin=12 V, Vo=1 V,  TON= 1.5 kΩ or 12.1 kΩ, Note **13** |  | 114 |  |
| Vin=12 V, Vo=1 V,  TON= 2.49 kΩ, or 14 kΩ, Note **13** |  | 91.5 |  |
| Vin=12 V, Vo=1 V,  TON= 3.48 kΩ, or 16.2 kΩ, Note **13** |  | 77 |  |

On Time ns

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Electrical specifications**

| **Symbol** | **Conditions** | **Min** | **Typ** | **Max** |
| --- | --- | --- | --- | --- |
| Ton | Vin=12 V, Vo=1 V,  TON= х.цф kΩ, or 18.7 kΩ, Note **13** |  | 66.5 |  |
| Vin=12 V, Vo=1 V,  TON= 5.76 kΩ, or 21.5 kΩ, Note **13** |  | 58.5 |  |
| Vin=12 V, Vo=1 V,  TON= 7.32 kΩ, or 24.9 kΩ, Note **13** |  | 52 |  |
| Vin=12V , Vo=1 V,  TON= 8.щшkΩ, or ущ.шkΩ, Note **13** |  | 47 |  |
| Vin=12V, Vo=1.0V,  TON = Floating, Note **13** |  | 114 |  |
| Ton (Min) | Vin=12 V, Vo=0 V |  | 23 | 32 |
| Toff (Min) | Tj=25 °C, VFB=0 V |  | 270 | 360 |

**Parameter Unit** On Time ns

Minimum On-Time ns Minimum Off-Time ns **VCC LDO Output**

| VCC | 5.5 V ۞ Vin ۞ 17 V,  when Icc =50 mA, Cload = 2.2 µF | 4.7 | 5.0 | 5.3 |
| --- | --- | --- | --- | --- |
| VCC\_drop | Vin = 4.3 V, Icc=50 mA, Cload=2.2 µF |  |  | 300 |
| Ishort | 5.5 V ۞ Vin ۞ 17 V |  | 90 |  |

Output Voltage V

VCC Dropout mV Short Circuit Current mA **Under Voltage Lockout**

| VCC\_UVLO\_Start | VCC Rising Trip Level | 3.8 | 4.0 | 4.2 |
| --- | --- | --- | --- | --- |
| VCC\_UVLO\_Stop | VCC Falling Trip Level | 3.6 | 3.8 | 4.0 |
| En\_UVLO\_Start | ramping up | 1.14 | 1.2 | 1.36 |
| En\_UVLO\_Stop | ramping down | 0.9 | 1 | 1.06 |
| REN |  | 500 | 1000 | 1500 |

VCC-Start Threshold V VCC-Stop Threshold V Enable-Start-Threshold V Enable-Stop-Threshold

Input Impedance kΩ **Over Current Limit**

Current Limit Threshold

| Ioc | Tj = 25 °C, int LDO, RILIM=24.9 kΩ | 33.9 | 39 | 45.0 |
| --- | --- | --- | --- | --- |
| Tj = 25 °C, int LDO, RILIM=21.5 kΩ | 28.3 | 32.5 | 37.4 |
| Tj = 25 °C, int LDO, RILIM=16.2 kΩ | 22.6 | 26 | 29.9 |
| Tj = 25 °C, int LDO, RILIM=ту.т kΩ | 15.0 | 19.5 | 23.0 |

(Valley current) A

**Over Voltage Protection**

| OVP\_Vth | FB Rising | 115 | 121 | 125 |
| --- | --- | --- | --- | --- |
| FB Falling, OVP hysteresis | 110 | 115 | 120 |
| OVP\_Tdly |  |  | 7 |  |
| Tblk\_Hiccup | Unlatched OVP |  | 20 |  |

OVP Trip Threshold % Vref

OVP Protection Delay µs Hiccup Blanking Time ms **Under Voltage Protection**

| UVP\_Vth | FB Falling | 65 | 70 | 75 |
| --- | --- | --- | --- | --- |
| UVP\_Tdly |  |  | 5 |  |
| Tblk\_Hiccup |  |  | 20 |  |

UVP Trip Threshold % Vref UVP Protection Delay µs Hiccup Blanking Time ms **Power Good**

| VPG(upper) | FB Rising | 85 | 91 | 95 |
| --- | --- | --- | --- | --- |

PGood Turn on Threshold % Vref

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Electrical specifications**

| **Symbol** | **Conditions** | **Min** | **Typ** | **Max** |
| --- | --- | --- | --- | --- |
| VPG(lower) | FB Falling | 80 | 84 | 90 |
| IPG | PG = 0.5 V, En = 2 V | 2.5 | 5 |  |
| VPG(low) | Vin = VCC =0 V, Rpull-up = 50 kΩ to 3.3 V |  | 0.3 | 0.5 |
| VPG(on)\_Dly | FB Rising, see VPG(upper) |  | 2.5 |  |
| VPG(comp)\_Dly | VFB < VPG(lower) or  VFB > VPG(upper) | 1 | 2 | 3.5 |
|  | PG = 3.3 V |  |  | 1 |

**Parameter Unit** PGood Turn off Threshold % Vref PGood Sink Current mA PGood Voltage Low V

PGood Turn on Delay ms PGood Comparator Delay µs

PGood Open Drain Leakage

Current µA **Thermal Shutdown**

|  | Note **11** |  | 140 |  |
| --- | --- | --- | --- | --- |
|  | Note **11** |  | 20 |  |

Thermal Shutdown °C Hysteresis

Note:

11. Guaranteed by construction and not tested in production

12. Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.

13. The Ton is trimmed so that the target switching frequency is achieved at around 10A load current using EVAL\_3889\_1Vout demo board.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Typical efficiency and power loss curves**

**8 Typical efficiency and power loss curves**

**8.1 PVin = Vin = ту V, fsw = чсс kHz**

PVin = Vin = 12 V, VCC = Internal LDO, Io = 0 A-30 A, fsw= 600 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3889, the inductor losses, the losses of the input and output capacitors, and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

**Table 1 Inductors for PVin = Vin = 12 V, fsw = 600 kHz**

| **Lout (nH)** | **P/N** | **DCR (m**Ω**)** |
| --- | --- | --- |
| 150 | HCB138380D-151 (Delta) | 0.15 |
| 150 | HCB138380D-151 (Delta) | 0.15 |
| 220 | FP1008R5-R220-R (Cooper) | 0.17 |
| 350 | HCBD101195-351(Delta) | 0.35 |
| 450 | HCBD101195-451(Delta) | 0.35 |

**Vo (V) Size (mm)** 1.0 12.4 x 8.3 x 8 1.2 12.4 x 8.3 x 8 1.8 10.8 x 8 x 8

3.3 10.1 x 11.4 x 9.5 5 10.1 x 11.4 x 9.5

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Typical efficiency and power loss curves**

**8.2 PVin = Vin = ту V, fsw = щсс kHz**

PVin = Vin = 12 V, VCC = Internal LDO, Io = 0 A-30 A, fsw = 800 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3889, the inductor losses, the losses of the input and output capacitors, and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

**Table 2 Inductors for PVin = Vin =12 V, fsw = 800 kHz**

| **Lout (nH)** | **P/N** | **DCR (m**Ω**)** |
| --- | --- | --- |
| 150 | HCB138380D-151 (Delta) | 0.15 |
| 150 | HCB138380D-151 (Delta) | 0.15 |
| 150 | HCB138380D-151 (Delta) | 0.15 |
| 350 | HCBD101195-351(Delta) | 0.35 |

**Vo (V) Size (mm)** 1.0 12.4 x 8.3 x 8 1.2 12.4 x 8.3 x 8 1.8 12.4 x 8.3 x 8 3.3 10.1 x 11.4 x 9.5

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Typical efficiency and power loss curves**

**8.3 PVin = Vin = ту V, fsw = тссс kHz**

PVin = Vin = 12 V, VCC = Internal LDO, Io = 0 A-30 A, fsw = 1000 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3889, the inductor losses, the losses of the input and output capacitors, and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

**Table 3 Inductors for PVin = Vin = 12 V, fsw = 1000 kHz**

| **Lout (nH)** | **P/N** | **DCR (m**Ω**)** |
| --- | --- | --- |
| 100 | AH3740A-100K (ITG) | 0.145 |
| 100 | AH3740A-100K (ITG) | 0.145 |
| 120 | AH3740A-120K (ITG) | 0.145 |

**Vo (V) Size (mm)** 1.0 6.4 x 9.5 x 10 1.2 6.4 x 9.5 x 10 1.8 6.4 x 9.5 x 10

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| --- |

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Typical efficiency and power loss curves**

**8.4 PVin = Vin = VCC = ц V, fsw = чсс kHz**

PVin = Vin = VCC = 5.0 V, Io = 0 A – 30 A, fsw = 600 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3889, the inductor losses, the losses of the input and output capacitors and and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

**Table 4 Inductors for PVin = Vin = VCC= 5 V, fsw = 600 kHz**

| **Lout (nH)** | **P/N** | **DCR (m**Ω**)** |
| --- | --- | --- |
| 120 | AH3740A-120K (ITG) | 0.145 |
| 120 | AH3740A-120K (ITG) | 0.145 |
| 150 | AH3740A-150K (ITG) | 0.145 |
| 150 | AH3740A-150K (ITG) | 0.145 |

**Vo (V) Size (mm)** 1.0 6.4 x 9.5 x 10 1.2 6.4 x 9.5 x 10 1.8 6.4 x 9.5 x 10 3.3 6.4 x 9.5 x 10

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Thermal De-rating curves**

**9 Thermal De-rating curves**

Measurement is done on Evaluation board of EVAL\_3889. PCB is a 6-layer board with 1.5 ounce Copper for top and bottom layer and 2 z Copper for the inner layers, FR4 material, size ф.с҅xф.75҅.

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| --- |

**Figure 4 Thermal de-rating curves, PVin = 12 V, Vo = 1.0 V/3.3 V/5 V, Fsw = 800 kHz, VCC = Internal LDO**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator RDS(ON) of MOSFET Over Temperature**

**10 RDSҙONҚ of MOSFET Over Temperature**

|  |
| --- |

**Figure 5 RDS(on) of MOSFETs over Junction Temperature**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Typical operating characteristics (-хс C ≤ Tj ≤ +туц CҚ**

**11 Typical operating characteristics ҙ-хс °C ≤ Tj ≤ +туц °CҚ**

|  |
| --- |

**Figure 6 Typical operating characteristics (set 1 of 3)**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Typical operating characteristics (-хс C ≤ Tj ≤ +туц CҚ**

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**Figure 7 Typical operating characteristics (set 2 of 3)**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Typical operating characteristics (-хс C ≤ Tj ≤ +туц CҚ**

|  |
| --- |

**Figure 8 Typical operating characteristics (set 3 of 3)**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Theory of operation**

**12 Theory of operation**

**12.1 Fast Constant On-Time Control**

The IR3889 features a proprietary Fast Constant On-Time (COT) Control, which can provide fast load transient response, good output regulation and minimize the design effort. Fast COT control compares the output voltage, Vo, to a floor voltage combined with an internal ramp signal. When Vo drops below that signal, a PWM signal is initiated to turn on the high-side FET for a fixed on-time. The floor voltage is generated from an internal compensated error amplifier, which compares the Vo with a reference voltage. Compared to the traditional COT control, Fast COT control significantly improves the Vo regulation.

**12.2 Enable**

En pin controls the on/off of the IR3889. An internal Under Voltage Lock-Out (UVLO) circuit monitors the En voltage. When the En voltage is above an internal threshold, the internal LDO starts to ramp up. When the VCC/LDO voltage rises above the VCC\_UVLO\_Start threshold, the soft-start sequence starts. The En pin can be configured in three ways, as shown in **Figure 9**. With configuration 2, the Enable signal is derived from the PVin voltage by a set of resistive divider, REN1 and REN2. By selecting different divider ratios, users can program a UVLO threshold voltage for the bus voltage. This is a very desirable feature because it prevents the IR3889 from operating until PVin is higher than a desired voltage level. For some space constrained designs, the En pin can be directly connected to PVin without using the external resistor dividers, as shown in Configuration 3. The En pin should not be left floating. A pull down resistor in the range of tens of kilohms is recommended. **Figure 10** illustrates the corresponding start-up sequences with three En configurations.

| PVin  PVin  PVin  PVin Vin  REN1  Vcc  PVin Vin  PVin Vin  En  Vcc  Vcc  IR3889  En IR3889  En IR3889  REN2            En = an external logic signal En = ோ��మ  ோ��భ+ோ��మ× ܲ௩�௡ PVin = Vin = En  Configuration 1 Configuration 2 Configuration 3 |
| --- |

**Figure 9 Enable Configurations**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Theory of operation**

| Pvin= Vin=12V  PVin=Vin=En=12V  Pvin = Vin = 12V  Vcc\_ UVLO  Vcc  Vcc  Vcc  En Threshold  Vcc\_UVLO  Vcc\_ UVLO  0V      0V  0V    0V  0V  En = REN2/(REN1+REN2)\*PVin  0V  En >1.2V  En Threshold  Fb  Fb  0V  Fb  0V  Pgood Turn-on  Pgood Turn-on  Pgood Turn-on  threshold  threshold  threshold  2.5ms  2.5ms  2.5ms  0V  0V  0V  PGood  PGood  PGood  0V  0V  0V        Pgood stays at logic low  Pgood stays at logic low  Pgood stays at logic low  En = an external logic signal En = ோ��మ  ோ��భ+ோ��మ× ܲ௩�௡ PVin = Vin = En  Configuration 1 Configuration 2 Configuration 3 |
| --- |

**Figure 10 Start-up sequence**

**12.3 FCCM and DEM Operation**

The IR3889 offers two operation modes: Forced Continuous Conduction (FCCM) and Diode Emulation Mode (DEM). With FCCM, the IR3889 always operates as a synchronous buck converter with a pseudo constant switching frequency and therefore achieves small output voltage ripples. In DEM, the synchronous FET is turned off when the inductor current is close to zero, which reduces the switching frequency and improves the efficiency at light load. At heavy load, both FCCM and DEM operate in the same way. The operation mode can be selected with TON/MODE pin, as shown in **Table 5**. It should be noted that the selection of the operation mode cannot be changed on the fly. To load a new TON/MODE configuration, En or VCC voltage needs to be cycled.

**12.4 Pseudo Constant Switching Frequency**

The IR3889 offers eight programmable switching frequencies, fsw, from 600 kHz to 2 MHz, by connecting an external resistor from TON/MODE pin to a quiet ground (AGND or PGND). Based on the selected fsw, the IR3889 generates the corresponding on-time of the Control FET for a given PVin and Vo, as shown by the formula below.

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Where fsw is the desired switching frequency. During the operation, the IR3889 monitors PVin and Vo, and can automatically adjust the on-time to maintain the pre-selected fsw. With the increase of the load, the switching frequency can increase to compensate for the power losses. Therefore, the IR3889 has a pseudo constant switching frequency.

Table 5 lists the resistors for TON/MODE pin. In this table, E96 resistors with ±1% tolerance are used. If E12 resistor values are preferred, please refer to the Section **12.15**. To load a new TON/MODE configuration, En or VCC voltage needs to be cycled.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Theory of operation**

**Table 5 Configuration Resistors for TON/MODE Pin**

**TON/MODE Resistor (kΩҚ**

| **Freq (kHz)** |
| --- |
| 600 |
| 800 |
| 1000 |
| 1200 |
| 1400 |
| 1600 |
| 1800 |
| 2000 |
| 600 |
| 800 |
| 1000 |
| 1200 |
| 1400 |
| 1600 |
| 1800 |
| 2000 |
| 800 |

**±1% Tolerance Mode** 0

1.5

2.49

3.48 4.53 5.76 7.32 8.87 10.5 12.1 14

16.2 18.7 21.5 24.9 28.7

FCCM DEM

Ton = Floating FCCM

**12.5 Soft-start**

The IR3889 has an internal digital soft-start to control the output voltage rise and to limit the current surge at the start-up. To ensure a correct start-up, the soft-start sequence initiates when the En and VCC voltages rise above their respective thresholds. The internal soft-start signal linearly rises from 0 V to 0.8 V in a defined time duration. The soft-start time does not change with the output voltage. During the soft-start, the IR3889 operates in DEM until 1ms after the output voltage ramps above the PGood turn-on threshold. The IR3889 has four soft-start time options selected by placing a resistor from SS/Latch pin to the ground. **Table 6** lists the resistor values and its corresponding soft-start time. In this table, E96 resistors with ±1% tolerance are used. If E12 resistor values are preferred, please refer to the Section **12.15**. For each soft-start time, there are two resistor options available. Please note that SS/Latch pin is a multi-function pin, which is also used to select different responses for Over Voltage Protection (OVP). Please note that to load a new SS/Latch selection, En or VCC voltage needs to be cycled.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Theory of operation**

**Table 6 Configuration Resistor for SS/Latch Pin**

**SS/Latch Resistor ҙkΩҚ**

| **Soft-start Time**  **(ms)** |
| --- |
| 1 |
| 2 |
| 4 |
| 8 |
| 1 |
| 2 |
| 4 |
| 8 |
| 4 |

**±1% Tolerance OVP** 0

4.53

1.5

5.76 2.49 7.32 3.48 8.87 10.5 18.7 12.1 21.5 14

24.9 16.2 28.7

Latch

No Latch

SS/Latch = Floating Latch

**12.6 Pre-bias Start-up**

The IR3889 is able to start up into a pre-charged output without causing oscillations and disturbances of the output voltage. When IR3889 starts up with a pre-biased output voltage, both control FET and Synch FET are kept off till the internal soft-start signal exceeds the FB voltage.

**12.7 Internal Low - Dropout ҙLDOҚ Regulator**

The IR3889 has an integrated low-dropout LDO regulator, providing the bias voltage for the internal circuitry. To minimize the standby current, the internal LDO is disabled when the En voltage is pulled low. Vin pin is the input of the LDO. When using the internal LDO for a single rail operation, Vin pin should be connected to PVin pin. To save the power losses on the LDO, an external bias voltage can be used by connecting Vin pin to the VCC/LDO pin. VDRV provides the bias voltage for the internal driver circuitry and should be shorted to VCC/LDO on the PCB. **Figure 11** illustrates the configuration of VCC/LDO, VDRV and Vin pin.

| Ext Vcc  PVin  PVin  4.7uF  PVin Vin  PVin Vin  VCC  VCC  VDRV  VDRV  IR3889  2.2uF ~10uF  10uF  IR3889  PGND  PGND      Single rail operation with the internal LDO Use an external VCC |
| --- |

**Figure 11 Configuration of Using the internal LDO or an external VCC.**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Theory of operation**

Section **7.1** specified the recommended operating voltage range of Vin and VCC under different configurations. Following design guidelines are recommended when configuring the VCC/LDO.

∙ Place a bypass capacitor to minimize the disturbance on the VCC and VDRV pin. For a single rail operation using the internal LDO, a 4.7 µF low ESR ceramic capacitor must be used between Vin pin and PGND and a 2.2 µF~10 µF low ESR ceramic capacitor is required to be placed close to the VCC/LDO and VDRV pin with reference to PGND. 10 µF MLCC is recommended for VCC bypass capacitor when Vin is below 5.5 V. When using an external VCC bias voltage, a 10 µF ceramic capacitor can be shared with Vin, VCC/LDO and VDRV pin.

∙ When using the internal LDO with 5.5 V ۞ Vin ۞ 17 V, it is recommended to check the required VCC bias current for the operation above 1.6 MHz, to ensure that it does not exceed the LDO output current capability as shown in **Figure 6**. With the increase of fsw, the resulting ICC is also increased mainly due to the increase of the gate charge that is proportional to fsw. In **Figure 6**, the typical ICC at PVin = Vin = 12 V and fsw = 800 kHz has been provided, which can be used to estimate the ICC at other fsw.

∙ For applications using the internal LDO with 4.3 V ۞ Vin ۞ ц.х V, the LDO can be in the dropout mode. It is important to ensure that the LDO voltage does not fall below the VCC UVLO threshold voltage. At Vin = 4.3 V, ICC must not exceed 50 mA under all operating conditions such as during a step-up load transient, in which the control loop may require the increase of fsw. OCP limits can be reduced due to the lower VCC voltage.

**12.8 Over Current Protection ҙOCPҚ**

The IR3889 offers cycle-by-cycle OCP response with four selectable current limits, which is set by the resistance at ILIM pin. The selected OCP limit bank is loaded to the IC during the power up and cannot be changed on the fly. To change the OCP limit, users must cycle En signal or VCC voltage. Cycle-by-cycle OCP response allows the IR3889 to fulfill a brief high current demand, such as a high inrush current during the start-up. The detailed operation is explained as follows.

The OCP is activated when En voltage is above its threshold. The OCP circuitry monitors the current of the Synchronous MOSFET through its Rds(on). When a new PWM pulse is requested by the control loop, if the current of Synchronous MOSFET exceeds the selected OCP limit, the IR3889 skips the PWM pulse and extends the on time of Synchronous MOSFET till the current drops below the OCP limit. The OCP operation is also illustrated in **Figure 12**. As can be seen, during OCP events, the valley of the inductor current is regulated around the OCP limit. But during the first switching cycle when the OCP is tripped, the valley of the inductor current can drop slightly below the OCP limit. It should be noted that OCP events do not pull the PGood signal low unless the Vo drops below the PGood turn-off threshold. If the OCP event persists, the output voltage can eventually drop below the Under Voltage Protection (UVP) threshold and trigger UVP. Then the IR3889 enters a hiccup mode.

The OCP limits are thermally compensated. Please refer to the typical performance of OCP limits in **Figure 7**and **Figure 8**. The OCP limits specified in the Section **7.2** refer to the valley of the inductor current when OCP is tripped. Therefore, the corresponding output DC current can be calculated as follows:

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Where: Iout\_OCP = Output DC current when OCP is tripped. ILIM = OCP limit specified in the Section **7.2**, which is the valley of inductor current. ΔiL = Peak-peak inductor ripple current.

To avoid the inductor saturation during OCP events, the following criterion is recommended for the inductor saturation current rating.

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Where: Isat is the inductor saturation current and ILIM\_max is the maximum spec of the OCP limit.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Theory of operation**

| OCP Tripped  Current  UVP Hiccup  Limit  Inductor  Pulse  Blanking  Current  skipped  time  HDrv  LDrv  PGood  UVP  Vo  Threshold  PGood Turn-off  Threshold |
| --- |

**Figure 12 Cycle-by-cycle OCP response**

**12.9 Under Voltage Protection ҙUVPҚ**

Under Voltage Protection (UVP) provides additional protection during OCP fault or other faults. UVP is activated when the soft-start voltage rises above 130 mV. UVP circuitry monitors the FB voltage. When it is below the UVP threshold for 5 µs (typical), an under voltage trip signal asserts and both Control MOSFET and Synchronous MOSFET are turned off. The IR3889 enters a hiccup mode with a blanking time of 20 ms, during which Control MOSFET and Synchronous MOSFET remain off. After the completion of blanking time, the IR3889 attempts to recover to the nominal output voltage with a soft-start, as shown in **Figure 12**. The IR3889 will repeat hiccup mode and attempt to recover until UVP condition is removed.

**12.10 Over Voltage Protection ҙOVPҚ**

Over Voltage Protection (OVP) is achieved by comparing the FB voltage to an OVP threshold voltage. When the FB voltage exceeds the OVP threshold, an over voltage trip signal asserts after 7 µs (typical) delay. Control MOSFET is latched off immediately and PGood flags low. Synchronous MOSFET remains on to discharge the output capacitor. When FB voltage drops below around 115% of the reference voltage, Synchronous MOSFET turns off to prevent the complete depletion of the output capacitors. **Figure 13** illustrates the OVP operation. The OVP comparator becomes active when the En signal is above the start threshold.

With SS/Latch pin, two OVP responses can be selected: Latch or No Latch, as shown in **Table 6**. With a latched OVP response, Control FET remains latched off until either VCC voltage or En signal is cycled. With an unlatched OVP response, the IR3889 enters a hiccup mode. Control FET remains off for a blanking time of 20ms. After hiccup blanking time expires, the IR3889 will try to restart with a soft-start. The IR3889 can stay in the hiccup mode infinitely if over voltage fault persists.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Theory of operation**

| HDrv  LDrv  121%Vref  115%Vref  Vref  OVP  91%Vref  91%Vref  84%Vref  VFB  PGood  Pgood turn-on  Pgood turn-on  OVP delay =7us  delay =2.5ms  delay =2.5ms |
| --- |

**Figure 13 Over voltage protection response and PGood behavior.**

**12.11 Over Temperature Protection ҙOTPҚ**

Temperature of the controller is monitored internally. When the temperature exceeds the over temperature threshold, OTP circuitry turns off both Control and Synchronous MOSFETs and resets the internal soft start. Automatic restart is initiated when the sensed temperature drops back into the operating range. The thermal shutdown threshold has a hysteresis of 20 °C.

**12.12 Power Good ҙPGoodҚ Output**

The PGood pin is the open drain of an internal NFET, and needs to be externally pulled high through a pull-up resistor. PGood signal is high when three criteria are satisfied.

1. En signal and VCC voltage are above their respective thresholds.

2. No over voltage and over temperature faults occur.

3. Vo is within the regulation.

In order to detect if Vo is in regulation, PGood comparator continuously monitors the FB voltage. When FB voltage ramps up above the upper threshold, PGood signal is pulled high after 2.5 ms. When FB voltage drops below the lower threshold, PGood signal is pulled low immediately. **Figure 13** illustrates the PGood response.

During the start-up with a pre-biased voltage, PGood signal is held low before the first PWM is generated and is then pulled high with 2.5 ms delay after FB voltage rises above the PGood threshold. IR3889 also integrates an additional PFET in parallel to the PGood NFET, as shown in **Figure 2**. This PFET allows PGood signal to stay at logic low when the VCC voltage is not present, and PGood pin is pulled up by an external bias voltage. Please refer to **Figure 10**. Since PGood PFET has relatively higher on resistance, a 50 kΩ pull-up resistor is needed for a PGood bias voltage of 3.3 V to maintain the PGood signal at logic low when PGood PFET is on.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Theory of operation**

**12.13 Minimum On - Time and Minimum Off - Time**

The minimum on-time refers to the shortest time for Control MOSFET to be reliably turned on. The minimum off time refers to the minimum time duration in which Synchronous FET stays on before a new PWM pulse is generated. The minimum off-time is needed for IR3889 to charge the bootstrap capacitor, and to sense the current of the Synchronous MOSFET for OCP.

For applications requiring a small duty cycle, it is important that the selected switching frequency results in an on-time larger than the maximum spec of the minimum on-time in the Section **7.2**. Otherwise the resulting switching frequency may be lower than the desired target. Following formula could be used to check for the minimum on-time requirement.

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Where fsw is the desired switching frequency. k is the variation of the switching frequency. As a rule of thumb, select k = 1.25 to ensure the design margin.

For applications requiring a high duty cycle, it is important to make sure a proper switching frequency is selected so that the resulting off-time is longer than the maximum spec of the minimum off-time in the Section **7.2**, which can be calculated as shown below.

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�݂௦௪ × ܲ��௡ሺ୫i୬ሻ௢௙௙ܶ ݂݋ �݁݌� max>

Where fsw is the desired switching frequency. k is the variation of the switching frequency. As a rule of thumb, select k = 1.25 to ensure the design margin.

The resulting maximum duty cycle is therefore determined by the selected on-time and minimum off-time.  ௫௠�ܦܶ௢௡

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**12.14 Selection of Feedforward Capacitor and Feedback Resistors**

Output voltage can be programmed with an external voltage divider. The FB voltage is compared to an internal reference voltage of 0.8 V. The divider ratio is set to provide 0.8 V at the FB pin when the output is at its desired value. The calculation of the feedback resistor divider is shown below.

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ܴி஻ଶሻ

Where RFB1 and RFB2 are the top and bottom feedback resistors.

A small MLCC capacitor, Cff, is preferred in parallel with the top feedback resistor, RFB1, to provide extra phase boost and to improve the transient load response, as shown in **Figure 14**. Following formula can be used to help select Cff and RFB1. The value of Cff is recommended to be 100 pF or higher to minimize the impact of circuit parasitic capacitance. **Table 7** lists the suggested m for some common outputs. Cff and RFB1 may be further optimized based on the transient load tests. Where Lo and Co are the output LC filter of the buck regulator.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Theory of operation**

| Vo  Cff FB  RFB1  RFB2 |
| --- |

**Figure 14 Configuration of feedforward capacitor, Cff.**

**Table 7 Selection of m**

**Vo m**

ф V ۞ Vo ۞ ц V 0.4

1.2 V < Vo < 3 V 0.6

Vo ۞ т.у V 0.8

**12.15 Resistors for Configuration Pins**

To properly configure SS/LATCH pin, MODE/TON pin and ILIM pin, E96 resistors with ±1% tolerance must be used per Table 5, Table 6 and Section **7.2**. If E12 resistor values are preferred, the E96 resistors can be replaced with two or three E12 resistors in series, as shown in Table 8. Note that the tolerance of E12 resistors must be ±0.1%.

**Table 8 Replacement of E96 configuration resistors with E12 resistors in series**

**E96 ±1% E12 ±0.1% (R = RS1 + RS2 or RS1 + RS2 + RS3)**

| RS1 ҙkΩҚ | RS2 ҙkΩҚ |
| --- | --- |
| 2.7 | 1.8 |
| 1.5 | 0 |
| 5.6 | 0.15 |
| 1.8 | 0.68 |
| 6.8 | 0.56 |
| 3.3 | 0.15 |
| 8.2 | 0.68 |
| 10 | 0.47 |
| 12 | 0.1 |
| 18 | 3.3 |
| 10 | 3.9 |
| 22 | 2.7 |
| 15 | 1.2 |
| 27 | 1.8 |
| 18 | 3.3 |
| 22 | 2.7 |

R ҙkΩҚ RS3 ҙkΩҚ

4.53 N/A

1.50 N/A

5.76 N/A

2.49 N/A

7.32 N/A

3.45 N/A

8.87 N/A

10.5 N/A

12.1 N/A

21.5 N/A

14 N/A

24.9 N/A

16.2 N/A

28.7 N/A

21.5 0.18

24.9 0.18

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Design example**

**13 Design example**

In this section, an example is used to explain how to design a buck regulator with the IR3889. The application

circuit is shown in Figure 15. The design specifications are given below.

∙ PVin = 12 V (±10%)

∙ Vo = 1.0 V

∙ Io = 30 A

∙ Vo ripple voltage = ±1% of Vo

∙ Load transient response = ± 3% of Vo with a step load current = 9 A and slew rate = 30 A/µs

**13.1 Enabling the IRфщщъ**

The IR3889 has a precise En threshold voltage, which can be used to implement a UVLO of the input bus voltage by connecting the En pin to PVin with a resistor divider, as shown in Configuration 2 of Figure 9. The En resistor divider, REN1 and REN2, can be calculated as follows.

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Where VEN(max) is the maximum spec of the En-start-threshold as defined in Section **7.2**. For PVin (min) =10.8 V, select REN1=49.9 kΩ and REN2=7.5 kΩ.

**13.2 Programming the Switching Frequency and Operation Mode**

The IR3889 has very good efficiency performance and is suitable for high switching frequency operation. In this case, 800 kHz is selected to achieve a good compromise between the efficiency, passive component size and dynamic response. In addition, FCCM operation is selected to ensure a small output ripple voltage over the entire load range. To select щсс kHz and FCCM operation, the TON/MODE pin can be left floating or connect a т.ц kΩ resistor to a quiet ground (AGND or PGND) per **Table 5**.

**13.3 Selecting Input Capacitors**

Without input capacitors, the pulse current of Control MOSFET is directly from the input supply power. Due to the impedance on the cable, the pulse current can cause disturbance on the input voltage and potential EMI issues. The input capacitors filter the pulse current, resulting in almost constant current from the input supply. The input capacitors should be selected to tolerate the input pulse current, and to reduce the input voltage ripple. The RMS value of the input ripple current can be expressed by:

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Where IRMS is the RMS value of the input capacitor current. Io is the output current and D is the Duty Cycle. For Io = 30A and D(max) = 0.09, the resulting RMS current flowing into the input capacitor is Irms = 8.7 A.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator Design example**

To meet the requirement of the input ripple voltage, the minimum input capacitance can be calculated as follows.

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Where ∆PVin is the maximum allowable peak-to-peak input ripple voltage, and ESR is the equivalent series resistor of the input capacitors. Ceramic capacitors are recommended due to low ESR, ESL and high RMS current capability. For Io = 30 A, fsw = щсс kHz, ESR = ф mΩ, and ∆PVin = 240 mV, Cin(min) > 18 µF. To account for the de rating of ceramic capacitors under a bias voltage, 10 x 22 µF/0805/25V MLCC are used for the input capacitors. In addition, a bulk capacitor is recommended if the input supply is not located close to the voltage regulator.

**13.4 Inductor Selection**

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value results in a large ripple current, lower efficiency and high output noise, but helps with size reduction and transient load response. Generally, the desired peak-to-peak ripple current in the inductor ҙ∆iҚ is found between 20% and 50% of the output current.

The inductor saturation current must be higher than the maximum spec of the OCP limit plus the peak-to-peak inductor ripple current. For some core material, inductor saturation current may decrease as the increase of temperature. So it is important to check the inductor saturation current at the maximum operating temperature.

The inductor value for the desired operating ripple current can be determined using the following relation: � = ሺܲ��௡ሺ୫axሻ − �௢ሻ ×௡�௠ܦ

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Where: PVin(max) = Maximum input voltage; ∆iLmax = Maximum peak-to-peak inductor ripple current; OCPmax = maximum spec of the OCP limit as defined in Section **7.2**; and Isat = inductor saturation current. In this case, select inductor L =150 nH to achieve ∆iLmax = 25% of Iomax. The Isat should be no less than 53 A.

**13.5 Output Capacitor Selection**

The output capacitor selection is mainly determined by the output voltage ripple and transient requirements. To satisfy the Vo ripple requirement, Co should satisfy the following criterion.

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Where ∆Vor is the desired peak-to-peak output ripple voltage. For ∆iLmax= 7.5 A, ∆Vor =20 mV, fsw = 800 kHz, Co must be larger than 59 µF. The ESR and ESL of the output capacitors, as well as the parasitic resistance or inductance due to PCB layout, can also contribute to the output voltage ripple. It is suggested to use Multi Layer Ceramic Capacitor (MLCC) for their low ESR, ESL and small size.

To meet the transient response requirements, the output capacitors should also meet the following criterion.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator Design example**

Where ∆VOL is the allowable Vo deviation during the load transient. ∆Io(max) is the maximum step load current. Please note that the impact of ESL, ESR, control loop response, transient load slew rate, and PWM latency is not considered in the calculation shown above. Extra capacitance is usually needed to meet the transient requirements. As a rule of thumb, we can triple the Co that is calculated above as a starting point, and then optimize the design based on the bench measurement. In this case, to meet the transient load requirement (i.e. ∆VOL= 30 mV, ∆Io(max) = 9 A), select Co = ~600 µF. For more accurate estimation of Co, simulation tool should be used to aid the design.

**13.6 Output Voltage Programming**

Output voltage can be programmed with an external voltage divider. The FB voltage is compared to an internal reference voltage of 0.8 V. The divider ratio is set to provide 0.8 V at the FB pin when the output is at its desired value. The calculation of the feedback resistor divider is shown below.

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Where RFB1 and RFB2 are the top and bottom feedback resistors. Select RFB1 = тч.у kΩ and RFB2 = чх.ъ kΩ, to achieve Vo = 1 V.

**13.7 Feedforward Capacitor**

A small MLCC capacitor, Cff, can be placed in parallel with the top feedback resistor, RFB1, to improve the transient response. Based on Section **12.14**, Cff can be selected using the following formula.

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With Lo = 150 nH, Co = 600 µF and RFB1 = тч.у kΩ, Cff= ~125 pF. Cffcan be further optimized on the bench test based on bode plot measurement and transient load response.

**13.8 Bootstrap Capacitor**

For most applications, a 0.1 µF ceramic capacitor is recommended for bootstrap capacitor placed between PHASE and BOOT Pin. For applications requiring PVin equal to or above 14 V, a small resistor of т~у Ω should be used in series with the BOOT pin to ensure the maximum SW node spike voltage does not exceed 20 V.

**13.9 Vin, VCC/LDO and VDRV bypass Capacitor**

Please see the recommendation in **Section 12.7**. A 10 µF MLCC is selected for VCC/LDO and VDRV bypass capacitor and a 4.7 µF MLCC is selected for Vin bypass capacitor.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Application Information**

**14 Application Information**

**14.1 Application Diagram**

| Cin  CinHF  10 x 22uF  4.7uF  Vin = 12V ±10%  + Optional  REN1  REN2  49.9k  7.5k  Cvin  4.7uF  RBoot  0  EN Vin PVin  Boot  CBoot  VCC/LDO  0.1uF  Phase  VDRV Vo=1V  RPG  Cvcc  SW  49.9k  10uF  L  PGood  + CoHF  Co1  Co2  150nH  NC  IR3889  PGood  0.1uF  1x470uF  9x47uF  GATEL  SS/Latch  RSS  Cff  Fb  Ton/Mode  1.5k  220pF  ILIM VSENM  RTon  NC NC NC  AGnd PGnd  RFB1  RFB2  1.5k  RLIM  16.2k  64.9k  24.9k |
| --- |

**Figure 15 Application diagram of IR3889. PVin = 12 V, Vo = 1V, Io = 30 A, fsw = 800 kHz. 14.2 Typical Operating Waveforms**

PVin = Vin = 12.0 V, Vo = 1 V, Io = 0 – 30 A, fsw = 800 kHz, Room Temperature, no airflow

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**Figure 16 Start up at 30 A Load, (Ch1: PVin, Ch2: Vo, Ch3:PGood ,Ch4:En)**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Application Information**

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**Figure 17 Pre-bias Start up at 0 A Load, (Ch1: PVin, Ch2: Vo, Ch3: PGood, Ch4: En)**

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**Figure 18 Vo ripple at 30 A Load, fsw = 800 kHz, (Ch1: Vo)**

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**Figure 19 SW node, 30 A load, fsw = 800 kHz**

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**30 A single-voltage synchronous Buck regulator**

**Application Information**

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**Figure 20 SW node (in DEM), 3.5 A load**

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**Figure 21 Short circuit and UVP (Hiccup), (Ch2: Vo, Ch3:PGood)**

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**Figure 22 Transient response at 9 A step load current @ 30 A/µs slew rate: Io= 16 A – 25 A, (Ch1: Vo, Ch4: Io), pk-pk: 60.8 mV, fsw = 800 kHz**

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**30 A single-voltage synchronous Buck regulator**

**Layout Recommendations**

**15 Layout Recommendations**

PCB layout is very important when designing high frequency switching converters. Layout will affect noise pickup

and can cause a good design to perform with less than expected results. Following design guidelines are recommended to achieve the best performance.

∙ Bypass capacitors, including input/output capacitors, Vin, VCC and VDRV bypass capacitors, should be placed near the corresponding pins as close as possible.

∙ Place bypass capacitors from IR3889 power input (Drain of Control MOSFET) to PGND (Source of Synchronous MOSFET) to reduce noise and ringing in the system. The output capacitors should be terminated to a ground plane that is away from the input PGND to mitigate the switching spikes on the Vo. The bypass capacitor shared by VCC and VDRV should be terminated to PGND.

∙ Place a boot strap capacitor near the IR3889 BOOT and PHASE pin as close as possible to minimize the loop inductance.

∙ SW node copper should only be routed on the top layer to minimize the impact of switching noises ∙ Connect AGND pin to the PGND pad through a single point connection. On the IR3889 demo board, AGND pin is connected to the exposed PGND pad with a copper trace.

∙ Via holes can be placed on PVin and PGND pads to aid thermal dissipation.

∙ Wide copper polygons are desired for PVin and PGND connections in favor of power losses reduction and thermal dissipation. Sufficient via holes should be used to connect power traces between different layers. ∙ Single-ended Vo sensing is often used for local sensing. To implement this configuration, following design guidelines should be followed, as illustrated in **Figure 23**.

o The output voltage can be sensed from a high-frequency bypass capacitor of 0.1 µF or higher, through a 15 mil PCB trace.

o Keep the Vo sense line away from any noise sources and shield the sense line with ground planes. o The sense trace is connected to a feedback resistor divider with the lower resistor terminated at VSENM pin.

o Short VSENM pin and AGND pin with a short trace.

∙ If it is required to sense the output voltage at a remote location, pseudo remoting sensing can be implemented as follows. The configuration is also shown in **Figure 24**.

o A pair of PCB traces with at least 15 mil trace width, running close to each other and away from any noise sources such as inductor and SW nodes, should be used to implement Kelvin sensing of the voltage across a high bypass capacitor of 0.1 µF or higher.

o The ground connection of the remote sensing signal must be terminated at VSENM pin. o The Vo connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor terminated at VSENM pin.

o Shield the pair of remote sensing lines with ground planes above and below.

o Do **NOT** connect VSENM pin and AGND pin in this configuration

∙ The En pin and configuration pins including SS/LATCH, TON/MODE, and ILIM should be terminated to a quiet ground. On the IR3889 standard demo board, they are terminated to the PGND copper plane away from the power current flow. Alternatively, they can be terminated to a dedicated AGND PCB trace.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator Layout Recommendations**

| 4.3V<Vin<17V  Enable  Vin PVin  EN  Boot  VCC/LDO  Phase  VDRV  Vo  SW  PGood  0.1uF  NC  IR3889  PGood  GATEL  SS/Latch  RFB1 Cff  Fb  Ton/Mode  ILIM VSENM  RFB2  NC NC NC  AGnd PGnd |
| --- |

**Figure 23 Single-ended Vo sense configuration**

| 4.3V<Vin<17V  Enable  Vin PVin  EN  Boot  VCC/LDO  Phase  VDRV  Vo  SW  PGood  0.1uF  NC  IR3889  PGood  GATEL  SS/Latch  Fb  Ton/Mode  Cff  A pair of Vo sense traces  ILIM VSENM  run close to each other.  NC NC NC  AGnd PGnd  RFB2 RFB1 |
| --- |

**Figure 24 Pseudo remote Vo sense configuration**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Layout Recommendations**

Following figures illustrate the PCB layout design of the IR3889 standard demo board with pseudo remote Vo

sense.

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**Figure 25 IR3889 Demo Board – Top Layer**

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**Figure 26 IR3889 Demo Board – Bottom Layer**

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| --- |

**Figure 27 IR3889 Demo Board – 2nd Layer (Ground)**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator Layout Recommendations**

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**Figure 28 IR3889 Demo Board – 3rd Layer (Ground & Signal)**

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**Figure 29 IR3889 Demo Board – 4th Layer**

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| --- |

**Figure 30 IR3889 Demo Board – 5th Layer**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Layout Recommendations**

**15.1 Solder Mask**

Evaluation has shown that the best overall performance is achieved using the substrate/PCB layout as shown in

the following figures. PQFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

Infineon recommends that larger Power or Land Area pads are Solder Mask Defined (SMD). This allows the underlying copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05 mm larger (on each edge) than the openings in the solder mask. This allows for layers to be misaligned by up to 0.1 mm on both axes. Ensure that the solder resist in-between the smaller signal lead areas is at least 0.15 mm wide, due to the high x/y aspect ratio of the solder mask strip.

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**Figure 31 Solder mask (all dimensions in mm)**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Layout Recommendations**

**15.2 Stencil Design**

In most cases, the thickness of a stencil has to be matched to the needs of all components on the PCB. For

typical integrated QFN or SON packages, stencils with a thickness of 100 µm to 120 µm are recommended. Further details and specific stencil design recommendations can be found in the application note ҄Recommendations for Board Assembly of Infineon Integrated Packages without Leads҅. A recommended stencil design is shown below. This design is for a stencil thickness of 100 µm.

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| --- |

**Figure 32 Stencil pad size and spacing (all dimensions in mm)**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator Package**

**16 Package**

This section includes marking, mechanical and packaging information for the IR3889.

**16.1 Marking Information**

| IR3889M PART NUMBER  DATA MATRIX CODE  LOT CODE  ASSEMBLY SITE CODE  PIN 1, IDENTIFIER DATE CODE, FORMAT YYWW |
| --- |

**Figure 33 Package Marking**

**16.2 Dimensions**

|  |
| --- |

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Package**

**Figure 34 Package Dimensions (all dimensions in mm)**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator Package**

**16.3 Tape and Reel Information**

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**Figure 35 Pin 1 orientation in the tape**

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Environmental Qualifications**

**17 Environmental Qualifications**

**Qualification Level Industrial**

|  | QFN Package |
| --- | --- |
| Human Body Model | ANSI/ESDA/JEDEC JS-001, 2 (2000 V to < 4000 V) |
| Charged Device Model | ANSI/ESDA/JEDEC JS-002, C3 (۟ |

Moisture Sensitivity JEDEC Level 2 @ 260 °C

ESD 1000 V) RoHS2 Compliant This product is in compliance with EU Directive 2015/863/EU amending Annex II to EU Directive 2011/65/EU (RoHS) and

contains Pb according RoHS exemption 7a, Lead in high

melting temperature type solders.

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**IRфщщъ OptiMOS™ IPOL**

**30 A single-voltage synchronous Buck regulator**

**Evaluation Boards and Support Documentation**

**18 Evaluation Boards and Support Documentation**

**Table 9 IR3889 Evaluation Boards and User Guides**

| **Specifications** |
| --- |
| 12 V±10%, 1 V, 30 A |
| 12 V±10%, 3.3 V, 30 A |

**Evaluation board Website Address** EVAL\_3889\_1Vout www.infineon.com/EVAL\_3889\_1Vout EVAL\_3889\_3.3Vout www.infineon.com/EVAL\_3889\_3.3Vout

**Table 10 IR3889 Package Information**

| **Package Type** |
| --- |
| PG-IQFN-36-2 |

**Device Website Address**

IR3889 https://www.infineon.com/cms/en/product/packages/PG-IQFN

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**IR3889 OptiMOSª IPOL**

**IR3889**

**Revision History**

IR3889

**Revision: 2022-04-11, Rev. 2.7**

Previous Revision

| Date |
| --- |
| 2019-06-14 |
| 2019-08-20 |
| 2019-10-21 |
| 2019-12-15 |
| 2020-01-23 |
| 2020-06-25 |
| 2021-07-27 |
| 2022-04-11 |

Revision Subjects (major changes since last revision)

2.0 Initial release

2.1(1) Update Fig 3 & 10; (2) clarify test conditions for SS and Ton and Update typical value of Ton; (3) Add OVP falling threshold; (4) Update IVFB spec from +/-0.4uA to +/-0.15uA; (5) Add VDRV spec to section 5 and 7.1; (6) Update ESD HBM spec;

2.2 Correct SS slew rate from 0.4mV/us to 0.2mV/us with SS = floating in EC table 2.3 Update Fig 2

2.4 (1) Update format; (2) Update Fig 2; (3) Correct units in Fig 7 & 8

2.5 (1) Clarify the RoHS compliance spec; (2) Update Junction-Case top thermal resistance;(3) Add Table 7

2.6(1) Add max Vout of 6V to the recommended operation conditions; (2) Update note 8; (3) Update Table 7; (4) Correct test condition of ILIM in EC table from VCC = 5V to int

LDO; (5) Update order info

2.7 (1) Update Figure 31, 32, 35; (2) Correct typos in test condition of dead band time

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